

Amendments to the Claims

Please amend the claims as follows. This listing of claims replaces all prior versions and listings of claims in the application:

1. (Currently Amended) A method of analyzing cells of a memory device, said method comprising the steps of:
 - applying voltages according to a first test pattern to nodes of a cell of said memory device;
 - applying voltages according to a second test pattern to said nodes of said cell of said memory device;
 - analyzing fail data for said cell of said memory device related to said first test pattern and said second test pattern;
 - determining a fail signature for said cell; and
 - determining a type of failure of said cell based upon the analysis of said fail data.
2. (Original) The method of claim 1 wherein said steps of applying voltages comprises steps of applying voltages to a node of a cell of a dynamic random access memory.
3. (Cancelled).
4. (Currently Amended) The method of claim 1 [[3]] further comprising a step of establishing a plurality of fail signatures, each fail signature being associated with a type of failure.
5. (Original) The method of claim 4 wherein said step of determining a type of failure comprises a step of comparing a fail signature of a cell to said plurality of fail signatures.

6. (Original) A method of analyzing cells of a memory device, said method comprising the steps of:
- establishing a plurality of fail signatures, each fail signature being associated with a type of failure;
 - applying voltages according to a plurality of test patterns to nodes of a cell of said memory device; analyzing fail data of said cell for said plurality of patterns;
 - determining a fail signature of said cell; and
 - determining a type of failure of said cell based upon said plurality of fail signatures.
7. (Original) The method of claim 6 wherein said step of establishing a plurality of fail signatures comprises a step of establishing fail signatures for nominal operation.
8. (Original) The method of claim 7 wherein said step of establishing a plurality of fail signatures for nominal operation comprises establishing fail signatures associated with complete failure of cells during nominal operation.
9. (Original) The method of claim 6 wherein said step of establishing a plurality of fail signatures comprises a step of establishing induced fail signatures.
10. (Original) The method of claim 9 wherein said step of establishing induced fail signatures comprises a step of establishing fail signatures indicating a leakage condition.
11. (Original) A method of analyzing cells of a memory device, said method comprising the steps of:
- establishing a plurality of fail signatures for said memory device, each fail signature being associated with a type of failure of a cell;
 - applying voltages according to a plurality of test patterns to nodes of a plurality of cells of said memory device;

analyzing fail data for said plurality of test patterns applied to said cells;
determining a fail signature of said plurality of cells;
comparing said fail signatures of said plurality of cells to said plurality of fail signatures; and
determining a type of failure for each failing cell of said plurality of cells.

12. (Original) The method of claim 11 wherein said step of establishing a plurality of fail signatures comprises a step of establishing fail signatures indicating failures during nominal operation.

13. (Original) The method of claim 11 wherein said step of establishing a plurality of fail signatures comprises a step of establishing fail signatures indicating leakage conditions.

14. (Original) The method of claim 11 further comprising a step of generating a first bit map having both hard fails and soft fails.

15. (Original) The method of claim 14 further comprising a step of generating a second bit map based upon said first bit map, said second bit map eliminating hard fails.

16. (Original) A system for analyzing cells of a memory device, said system comprising:

a plurality of probes applying different test voltages to a cell of said memory device;

a control circuit varying the voltages applied to said cell, said control circuit comparing the failures of said cell as the test voltages applied to said cell are varied to an artificial bit fail map; and

an output device generating an output indicating a type of failure of said cell.

17. (Original) The system of claim 16 wherein said control circuit varies the voltage applied to said cell according to a plurality of test patterns.

18. (Original) The system of claim 16 wherein said plurality of probes apply test voltages to a plurality of cells.

19. (Original) The system of claim 16 wherein said output device comprises a printer.

20. (Original) The system of claim 16 wherein said output device comprises a display.